

Figure 1.

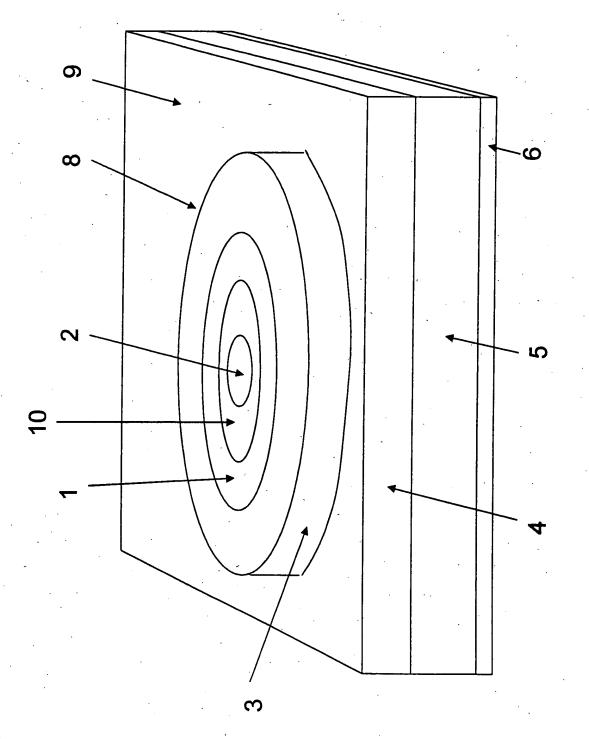


Figure 2.

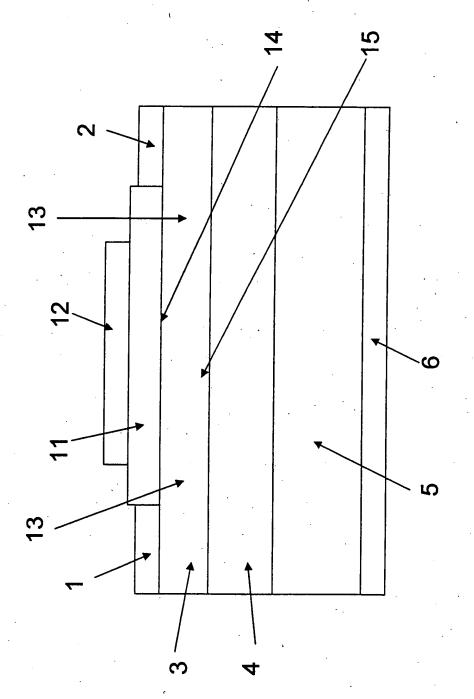


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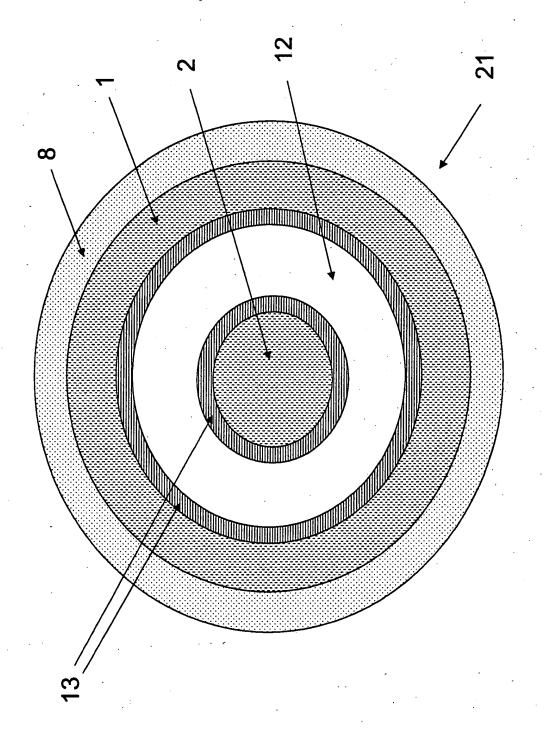


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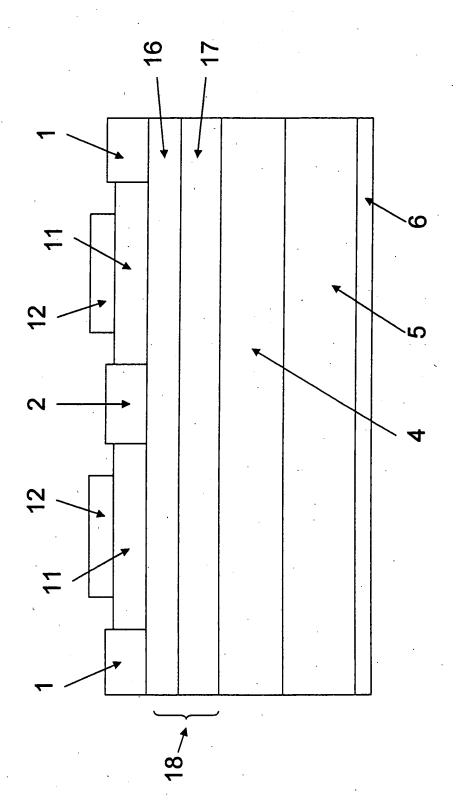


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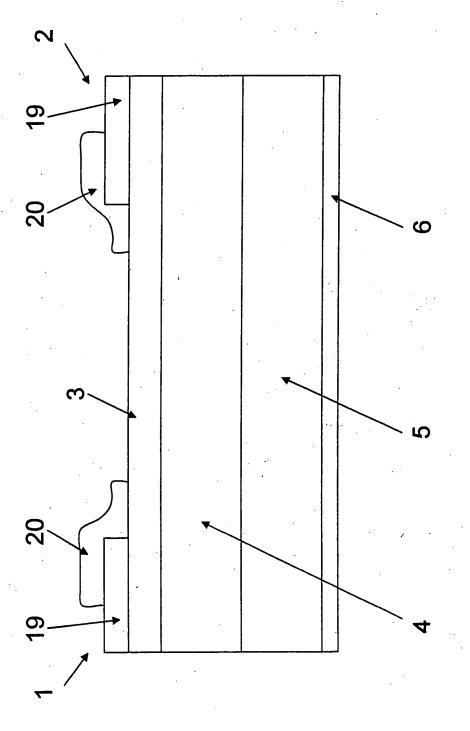
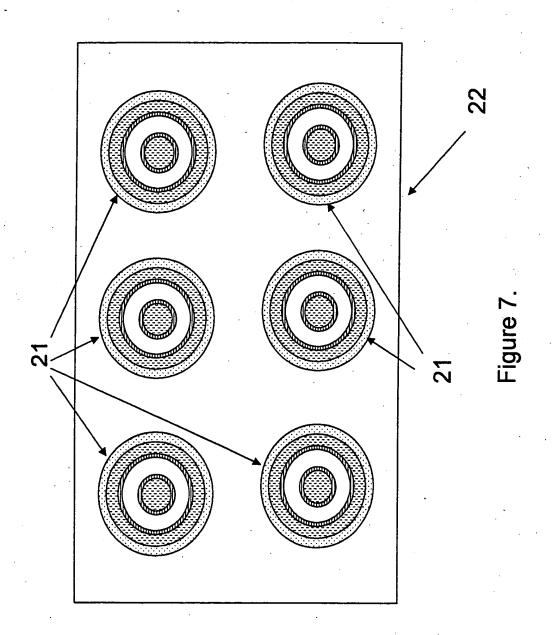


Figure 6.



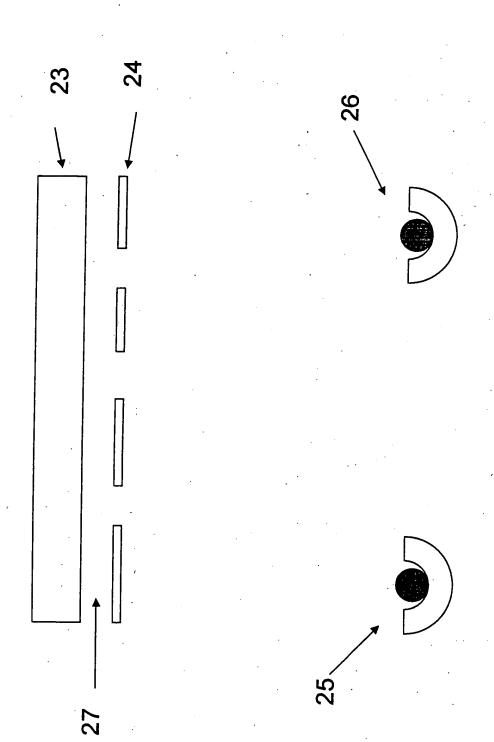


Figure 8.

PROVIDING A GATE INSULATOR ON A SURFACE OF THE SEMICONDUCTOR LAYER OR OF THE STRAINED SI LAYER

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DEPOSITING SOURCE AND DRAIN METAL ELECTRODES IN A GEOMETRIC PATTERN, INCLUDING DEPOSITING A FIRST METAL ELECTRODE LAYER FROM THE GROUP CONSISTING OF A1, Er, Gd, Nd, Ti, AND Y, FOLLOWED BY DEPOSITING A SECOND METAL LAYER FROM THE GROUP CONSISTING OF Ag, A1, Au, Cr, Cu, Ni AND Pt, TO FORM AN ELECTRODE STRUCTURE

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ANNEALING THE ELECTRODE STRUCTURE AT AN ELEVATED TEMPERATURE IN AN INERT ATMOSPHERE

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DEPOSITING A GATE ELECTRODE ON THE GATE INSULATOR BETWEEN THE SOURCE AND DRAIN METAL ELECTRODES WITHOUT CONTACTING THE SOURCE AND DRAIN METAL ELECTRODES

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DEPOSITING A PROTECTIVE LAYER OF PHOTORESIST OVER THE ENTIRE Si SURFACE

-115

COVERING THE PROTECTIVE LAYER OF PHOTORESIST WITH A METAL LAYER EVAPORATED THROUGH A MASK TO FORM A PROTECTIVE MASK TO COVER AND MASK THE INDIVIDUAL ISOLATED MESAS

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CREATING INDIVIDUAL ISOLATED MESAS, AS AN ARRAY OF INDIVIDUAL TEST MESA STRUCTURES, OF THE PROTECTIVE LAYER TO FORM A PROTECTIVE MASK LAYER ON THE SI SURFACE WITH THE SOURCE, DRAIN, AND GATE ELECTRODES RESIDING WITHIN THE BOUNDARIES OF THE MESAS:

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REMOVING THE GATE INSULATOR AND THE SEMICONDUCTOR LAYERS IN REGIONS BETWEEN THE MEASAS

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REMOVING THE PROTECTIVE MASK LAYER

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IRRADIATING A SI SURFACE OF THE TEST DEVICE WITH LIGHT HAVING A WAVELENGTH SHORTER THAN THE BANDGAP WAVELENGTH OF THE SI SURFACE

